ABSTRACT OF THE DISCLOSURE

An FCRAM includes first to third circuits. The first circuit generates a first signal based on a command detection signal. The second circuit is configured to receive the command detection signal, an operation mode specifying signal and a selection signal and generate a second signal which causes the start timing of the operation of a row-system circuit to be synchronized with the input timing of a second command. The third circuit is configured to select the first signal when a normal operation mode is specified by the operation mode specifying signal, select the second signal when a test mode is specified, and generate a third signal used to activate at least part of the memory cells in a memory cell array based on a selected one of the first and second signals and the selection signal.